

ABSTRACT OF THE DISCLOSURE

A semiconductor integrated circuit device includes a plurality of first memory cells each of which includes a cell transistor whose gate terminal is connected to a word line and a ferroelectric capacitor which is connected at one end to a source terminal of the cell transistor. The drain terminals of the cell transistors are used as a first local bit line, the other end of each of the ferroelectric capacitors are used as a first plate line. A first reset transistor has a source terminal connected to the first plate line and a drain terminal connected to the first local bit line. A first block selection transistor has a source terminal connected to the first local bit line and a drain terminal connected to a first bit line.